DESPEC DSSD Working Group Status & Open Issues

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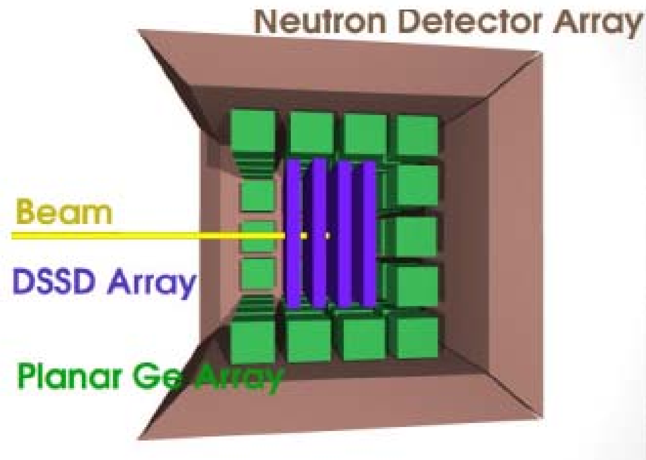
School of Physics

Concept



- Super FRS Low Energy Branch (LEB)
- Exotic nuclei – energies ~50-150MeV/u
- Implanted into multi-plane DSSD array
- Implant - decay correlations
- Multi-GeV DSSD implantation events
- Observe subsequent p, 2p, α, β, γ, βp, βn … decays
- Measure half lives, branching ratios, decay energies …

Configurations

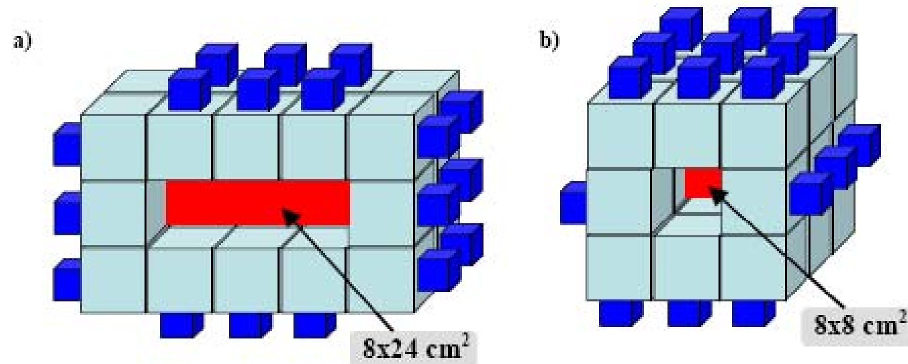


Fig. 13: Possible geometries of the proposed Ge array consisting of 24 detector units.

Two configurations proposed:

a) 8cm x 24cm
"cocktail" mode
many isotopes measured simultaneously

b) 8cm x 8cm
high efficiency mode
concentrate on particular isotope(s)

DSSD Segmentation

We need to implant at high rates *and* to observe implant – decay correlations for decays with long half lives.

DSSD segmentation ensures average time between implants for given *x,y* quasi-pixel >> decay half life to be observed.

- Implantation profile

  $\sigma_x \sim \sigma_y \sim 2cm$

  $\sigma_z \sim 1mm$
- Implantation rate (8cm x 24cm) ~ 10kHz, ~kHz per isotope (say)
- Longest half life to be observed ~ seconds

Implies quasi-pixel dimensions ~ 0.5mm x 0.5mm

Segmentation also has instrumentation performance benefits

DSSD

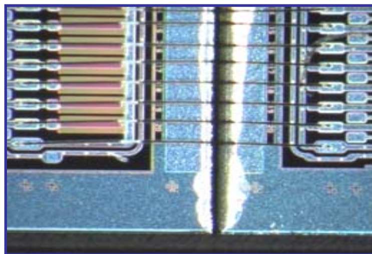
Technology well established
(e.g. GLAST LAT tracker)

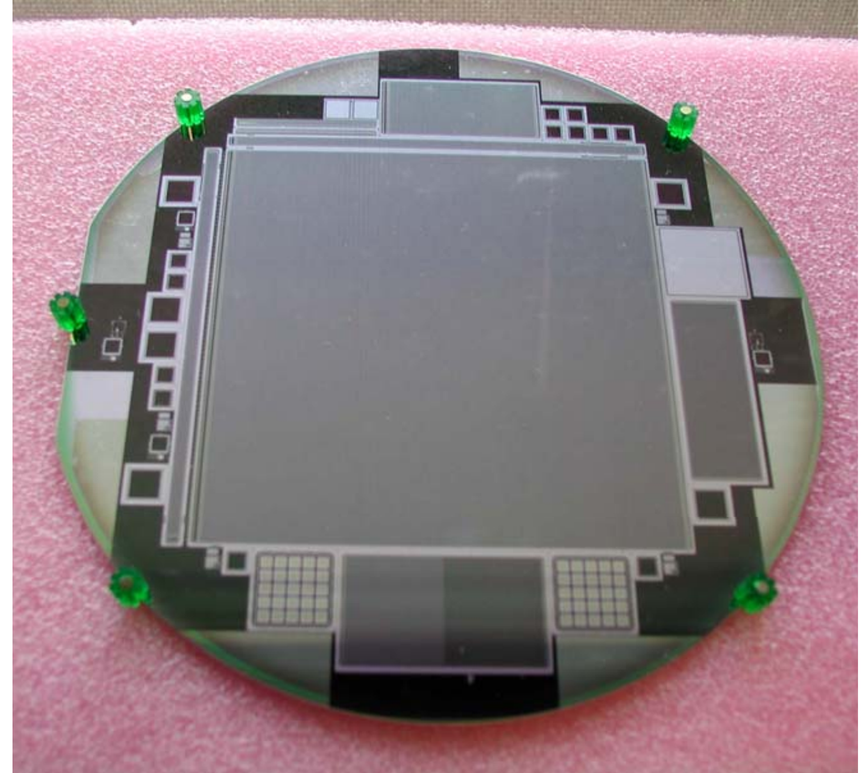
- 6" wafer technology
  10cm x 10cm area

- 1mm wafer thickness

- Integrated components
  a.c. coupling
  polysilicon bias resistors
  … important for ASICs

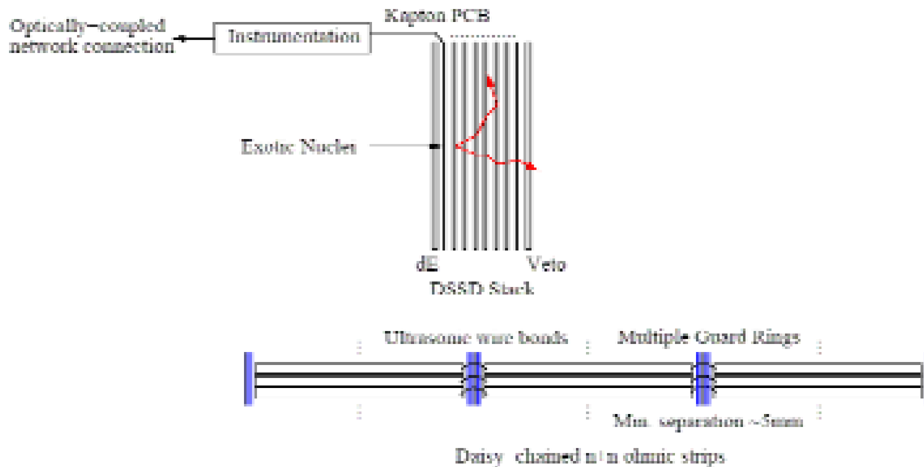
- Series strip bonding





8.95 cm square Hamamatsu-Photonics SSD before cutting from the 6-inch wafer. The thickness is 400 microns, and the strip pitch is 228 microns.

DSSD Array Design



Implantation depth?
Stopping power?
Ge β detector?
Calibration?

- 8cm x 8cm DSSDs
  - *common wafer design* for 8cm x 24cm and 8cm x 8cm configurations
- 8cm x 24cm
  - 3 adjacent wafers – horizontal strips series bonded
- 128 p+n junction strips, 128 n+n ohmic strips per wafer
- strip pitch 625μm
- wafer thickness 1mm
- ΔE, Veto and 6 intermediate planes
  - 4096 channels (8cm x 24cm)
- overall package sizes (silicon, PCB, connectors, enclosure …)
  - ~ 10cm x 26cm x 4cm or ~ 10cm x 10cm x 4cm

Instrumentation

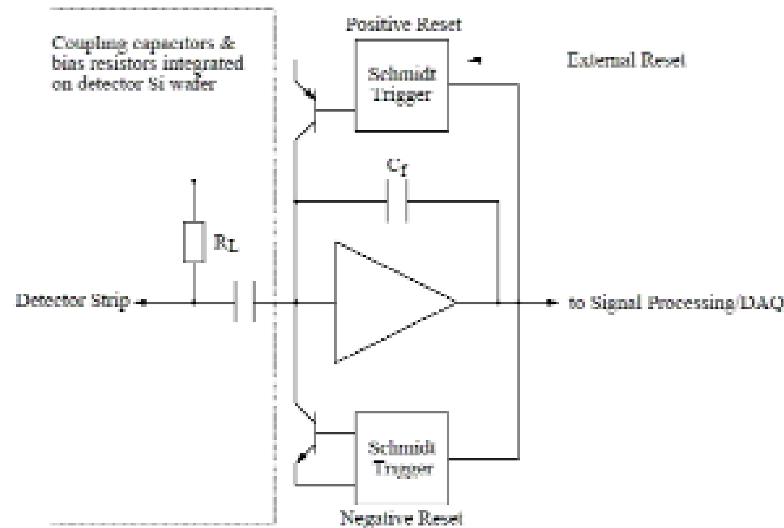
Large number of channels required, limited available space and cost *mandate* use of Application Specific Integrated Circuit (ASIC) technology.

Capabilities

- Selectable gain: low 20GeV FSR : high 20MeV FSR
- Noise σ ~ 5keV rms.
- Selectable threshold: minimum ~ 25keV @ high gain (assume 5σ)
- Integral and differential non-linearity
- Autonomous overload recovery ~μs
- Signal processing time <10μs (decay-decay correlations)
- Receive timestamp data
- Timing trigger for coincidences with other detector systems

DSSD segmentation reduces input loading of preamplifier and enables excellent noise performance.

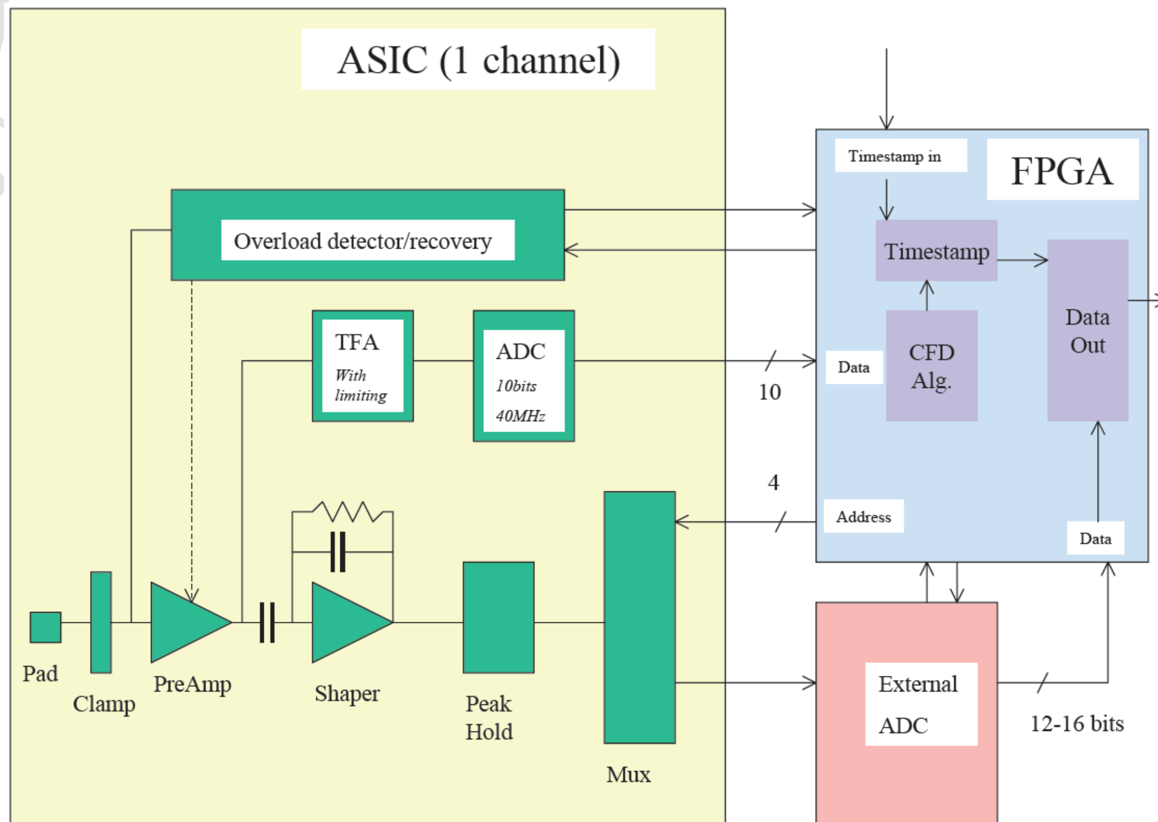
Instrumentation contd.



Preamplifier overload recovery *per* D.A.Landis *et al*., IEEE NS 45 (1998) 805

Originally developed for spaceborne HPGe detectors – possible application for back detectors of DESPEC γ-ray detector array?

ASIC *Concept*



- *Example* design concept
- Integrated DAQ
- Digital data via fibre-optic cable to PC-based data concentrator/event builder

Courtesy Ian Lazarus (CCLRC Daresbury Laboratory)

Current Status

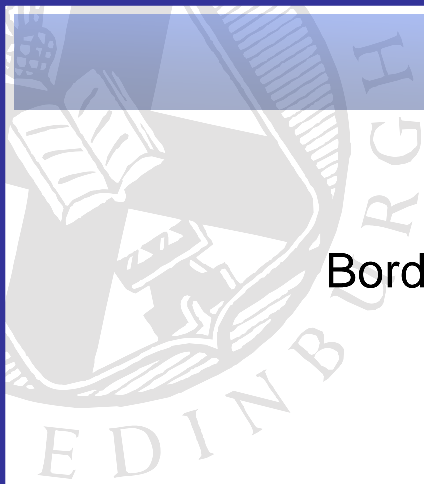
- Edinburgh – Liverpool – CCLRC DL – CCLRC RAL collaboration to submit joint grant bid to UK EPSRC at beginning of July 2005

  - 4 year grant period
  - DSSD design, prototype and production
  - ASIC design, prototype and production
  - Integrated Front End PCB development and production
  - Systems integration
  - Software development

Deliverable: fully operational DSSD array to DESPEC

- Physics Prioritisation panel meeting October 2005

- *If* approved
  - *detailed* specification development commences
  - specification finalised and critical review 2006/Q2 (M0)
  - funds available 2006/Q2



Working Group

Bordeaux – Bucharest – Edinburgh – Liverpool - Munich

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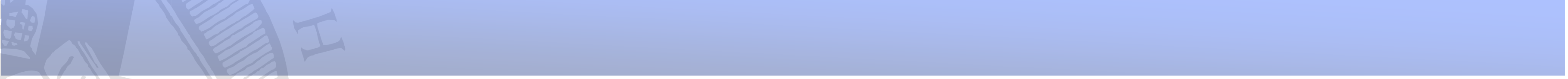

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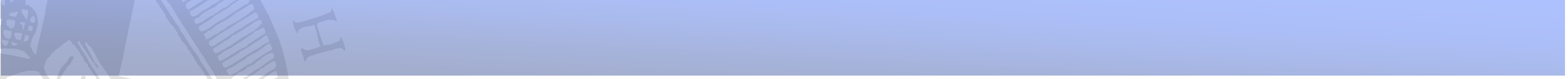

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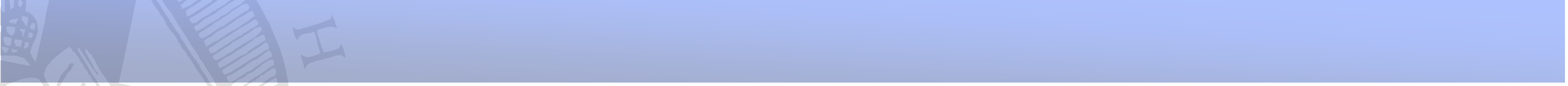

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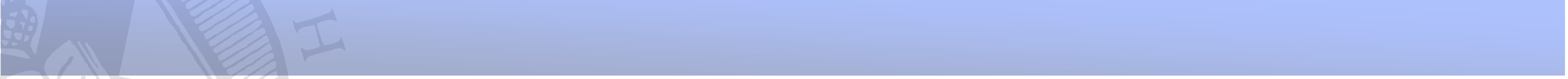

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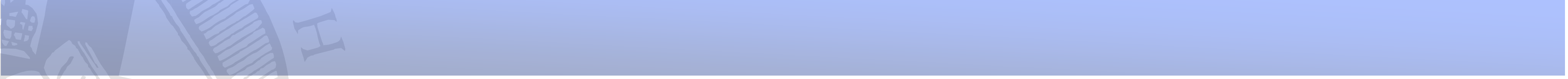

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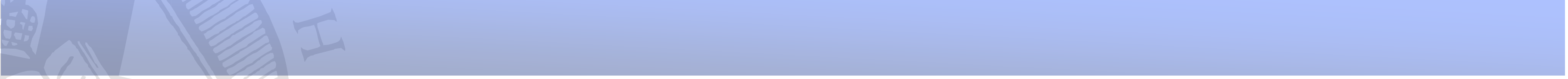
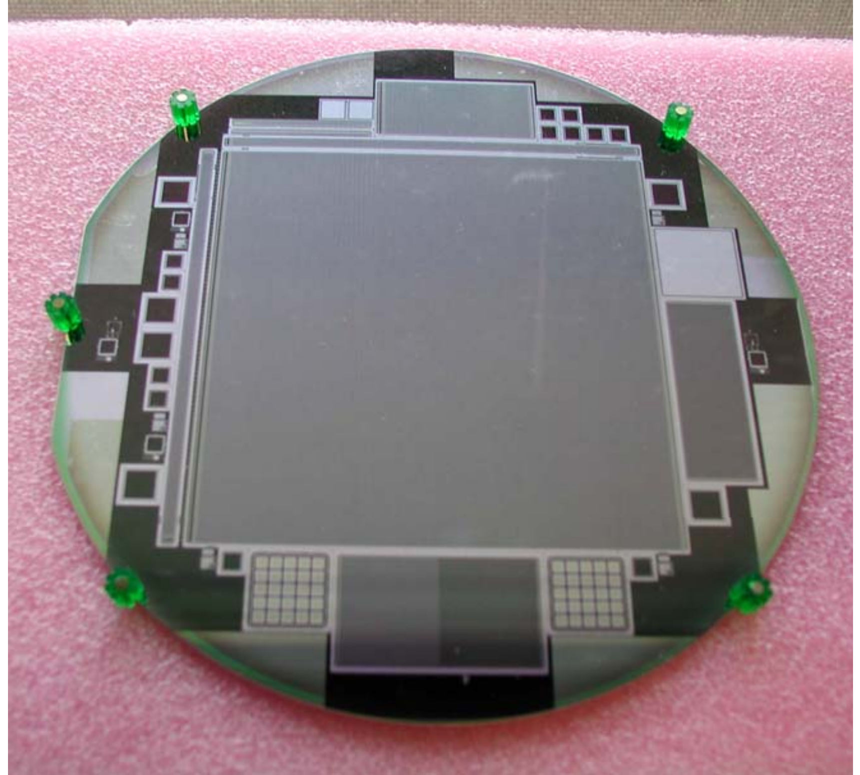


Silicon-Strip Detectors

- ~80 m^2 of PIN diodes, with *P* implants segmented into narrow strips.
- Reliable, well-developed technology from particle-physics applications.
- A/C coupling and



8.95 χμ σθυαρε Ηαμαματσυ– Πηοτονιχσ ΣΣΔ βεφορε χυττινγ φρομ τηε 6–ινχη ωαφερ. Τηε τηιχκνεσσ ισ 400 μιχρονσ, ανδ τηε στριπ πιτχη ισ 228 μιχρονσ.

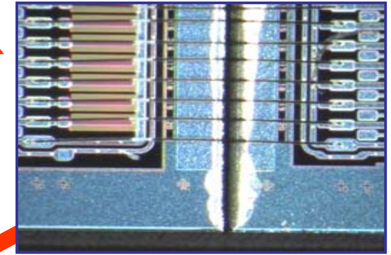
Electronics Packaging

Carbon composite side panels

Tested SSDs procured from Hamamatsu Photonics

10,368

4 SSDs bonded in series.



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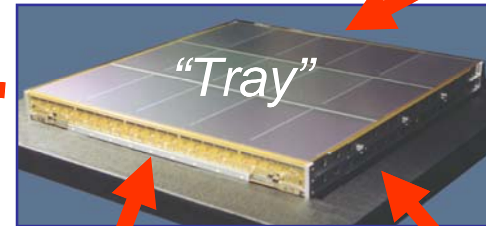
19 “trays” stack to form one of 16 Tracker modules.



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Electronics and SSDs assembled on composite panels.

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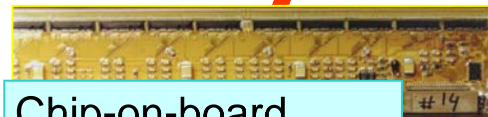

Chip-on-board readout electronics modules.

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Composite panels, with tungsten foils bonded to the bottom face.

Kapton readout cables.

Electronics mount on the tray edges.